

## Monolithic Quad SPST CMOS Analog Switches

February 1995

### Features

- ON-Resistance 85Ω Max
- Low Power Consumption ( $P_D < 35\mu W$ )
- Fast Switching Action
  - $t_{ON} < 250ns$
  - $t_{OFF} < 120ns$  (DG444)
- Low Charge Injection
- Upgrade from DG211/DG212
- TTL, CMOS Compatible
- Single or Split Supply Operation

### Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

### Description

The DG444 and DG445 monolithic CMOS analog switches are drop-in replacements for the popular DG211 and DG212 series devices. They include four independent single pole single throw (SPST) analog switches and TTL and CMOS compatible digital inputs.

These switches feature lower analog ON resistance ( $< 85\Omega$ ) and faster switch time ( $t_{ON} < 250ns$ ) compared to the DG211 and DG212. Charge injection has been reduced, simplifying sample and hold applications.

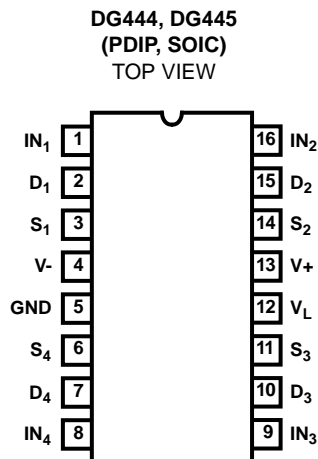
The improvements in the DG444 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling  $\pm 20V$  signals when operating with  $\pm 20V$  power supplies.

The four switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a  $\pm 5V$  analog input range. The switches in the DG444 and DG445 are identical, differing only in the polarity of the selection logic.

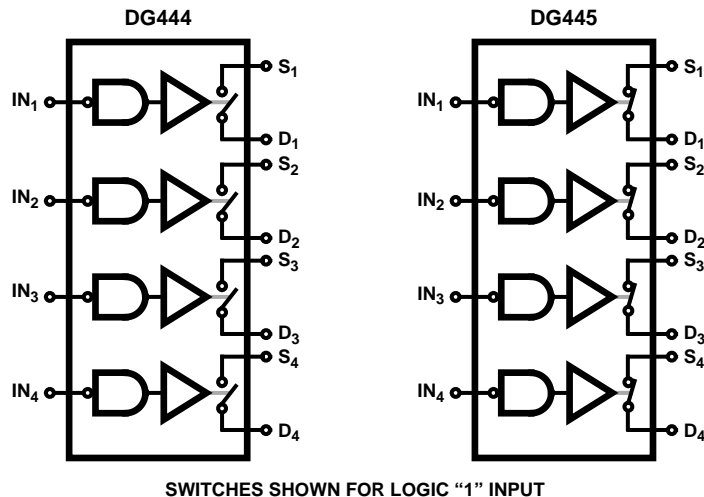
### Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG444DJ	-40°C to +85°C	16 Lead Plastic DIP
DG444DY	-40°C to +85°C	16 Lead SOIC (N)
DG445DJ	-40°C to +85°C	16 Lead Plastic DIP
DG445DY	-40°C to +85°C	16 Lead SOIC (N)

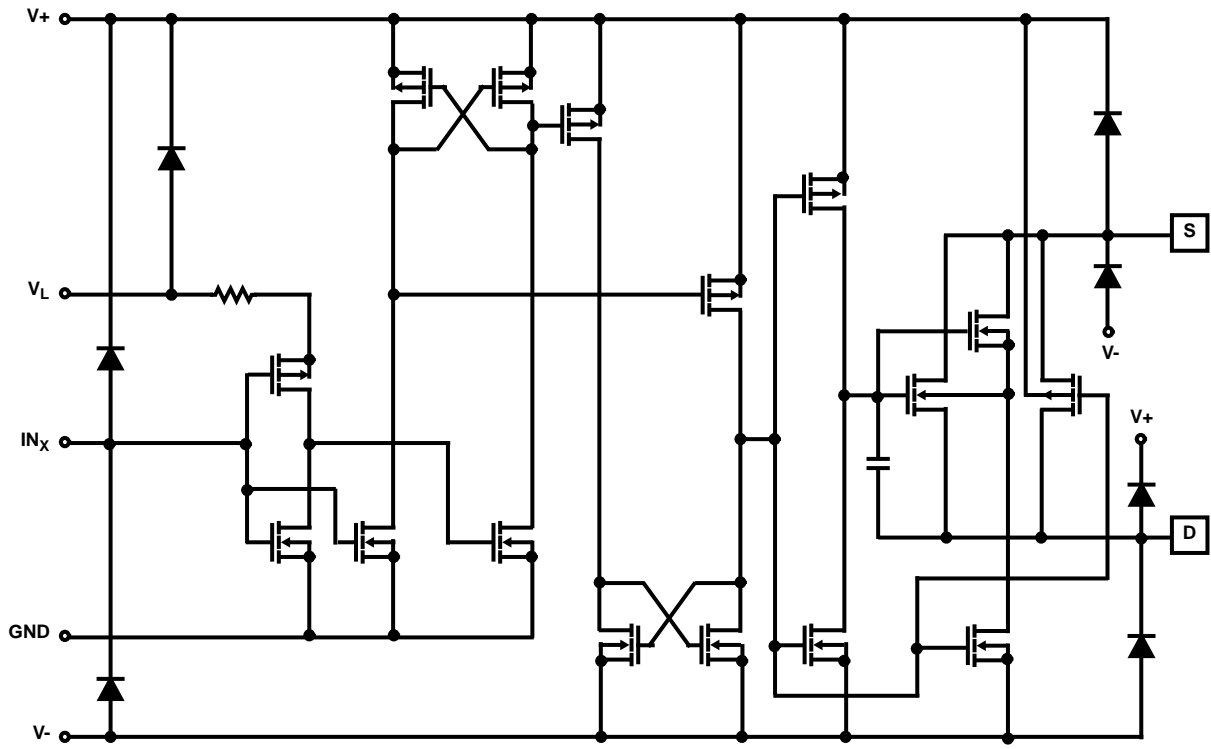
### Pinout



### Functional Diagrams



Typical Schematic Diagram (One Channel)



# Specifications DG444, DG445

## Absolute Maximum Ratings

V+ to V-	44V
GND to V-	25V
V <sub>L</sub>	(GND - 0.3V) to (V+) + 0.3V
Digital Inputs, V <sub>S</sub> , V <sub>D</sub> (Note 1)	(V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous Current (Any Terminal)	30mA
Current, S or D (Pulsed 1ms, 10% Duty Cycle)	100mA
Storage Temperature Range (D Suffix)	-65°C to +150°C

## Thermal Information

Thermal Resistance (Note 3)	$\theta_{JA}$
Plastic DIP Package	145°C/W
SOIC Package	115°C/W
Operating Temperature (D Suffix)	-40°C to +85°C
Junction Temperature (PDIP, SOIC)	+150°C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## Operating Conditions

Operating Voltage Range	±20V Max	Input High Voltage	2.4V Min
Operating Temperature Range	-55°C to +125°C	Input Rise and Fall Time	≤20ns
Input Low Voltage	0.8V Max		

## Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V<sub>L</sub> = 5V, V<sub>IN</sub> = 2.4V, 0.8V (Note 3),  
Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP	D SUFFIX -40°C TO +85°C			UNITS
			(NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	
<b>DYNAMIC CHARACTERISTICS</b>						
Turn-ON Time, T <sub>ON</sub>	R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 35pF, V <sub>S</sub> = ±10V, (See Figure 18)	+25°C	-	120	250	ns
Turn-OFF Time, T <sub>OFF</sub>		+25°C	-	110	140	ns
DG444		+25°C	-	160	210	ns
Charge Injection, Q	C <sub>L</sub> = 1nF, V <sub>S</sub> = 0V, V <sub>GEN</sub> = 0V, R <sub>GEN</sub> = 0Ω	+25°C	-	-1	-	pC
OFF Isolation	R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF, f = 1MHz	+25°C	-	60	-	dB
Crosstalk (Channel-to-Channel)	Any Other Channel Switches R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF, f = 1MHz	+25°C	-	100	-	dB
Source OFF Capacitance, C <sub>S(OFF)</sub>	f = 1MHz	+25°C	-	4	-	pF
Drain OFF Capacitance, C <sub>D(OFF)</sub>	f = 1MHz	+25°C	-	4	-	pF
Channel ON Capacitance, C <sub>D(ON)</sub> + C <sub>S(ON)</sub>	V <sub>ANALOG</sub> = 0	+25°C	-	16	-	pF
<b>DIGITAL CONTROL</b>						
Input Current V <sub>IN</sub> Low, I <sub>IL</sub>	V <sub>IN</sub> Under Test = 0.8V, All Others = 2.4V	Full	-0.5	-0.00001	0.5	μA
Input Current V <sub>IN</sub> High, I <sub>IH</sub>	V <sub>IN</sub> Under Test = 2.4V, All Others = 0.8V	Full	-0.5	0.00001	0.5	μA
<b>ANALOG SWITCH</b>						
Analog Signal Range, V <sub>ANALOG</sub>		Full	-15	-	15	V
Drain-Source ON Resistance, R <sub>DS(ON)</sub>	I <sub>S</sub> = -10mA, V <sub>D</sub> = ±8.5V, V+ = 13.5V, V- = -13.5V	+25°C	-	50	85	Ω
		Full	-	-	100	Ω
Switch OFF Leakage Current, I <sub>S(OFF)</sub>	V+ = 16.5V, V- = -16.5V, V <sub>D</sub> = ±15.5V, V <sub>S</sub> = ±15.5V	+25°C	-0.5	0.01	0.5	nA
		Hot	-5	-	5	nA
Switch OFF Leakage Current, I <sub>D(OFF)</sub>	V+ = 16.5V, V- = -16.5V, V <sub>D</sub> = ±15.5V, V <sub>S</sub> = ±15.5V	+25°C	-0.5	0.01	0.5	nA
		Hot	-5	-	5	nA
Channel ON Leakage Current, I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V+ = 16.5V, V- = -16.5V V <sub>S</sub> = V <sub>D</sub> = ±15.5V	+25°C	-0.5	0.08	0.5	nA
		Hot	-10	-	10	nA

## Specifications DG444, DG445

**Electrical Specifications** Test Conditions:  $V_+ = +15V$ ,  $V_- = -15V$ ,  $V_L = 5V$ ,  $V_{IN} = 2.4V, 0.8V$  (Note 3),  
Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP	D SUFFIX -40°C TO +85°C			UNITS
			(NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	
POWER SUPPLIES						
Positive Supply Current, $I_+$	$V_+ = 16.5V$ , $V_- = -16.5V$ , $V_{IN} = 0V$ or $5V$	+25°C	-	0.001	1	$\mu A$
		Hot	-	-	5	$\mu A$
Negative Supply Current, $I_-$		+25°C	-1	-0.0001	-	$\mu A$
		Hot	-5	-	-	$\mu A$
Logic Supply Current, $I_L$		+25°C	-	0.001	1	$\mu A$
		Hot	-	-	5	$\mu A$
Ground Current, $I_{GND}$	+25°C	-1	-0.001	-	$\mu A$	
	Hot	-5	-	-	$\mu A$	

**Electrical Specifications** (Unipolar Supplies) Test Conditions:  $V_+ = +12V$ ,  $V_- = 0V$ ,  $V_L = 5V$ ,  $V_{IN} = 2.4V, 0.8V$  (Note 3),  
Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP	D SUFFIX -40°C TO +85°C			UNITS
			(NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	
DYNAMIC CHARACTERISTICS						
Turn-ON Time, $T_{ON}$	$R_L = 1k\Omega$ , $C_L = 35pF$ , $V_S = 8V$ , (See Figure 18)	+25°C	-	300	450	ns
Turn-OFF Time, $T_{OFF}$		+25°C	-	60	200	ns
Charge Injection, $Q$	$C_L = 1nF$ , $V_{GEN} = 6V$ , $R_{GEN} = 0\Omega$	+25°C	-	2	-	pC
ANALOG SWITCH						
Analog Signal Range, $V_{ANALOG}$		Full	0	-	12	V
Drain-Source ON Resistance, $R_{DS(ON)}$	$I_S = -10mA$ , $V_D = 3V, 8V$ $V_+ = 10.8V$ , $V_L = 5.25V$	+25°C	-	100	160	$\Omega$
		Full	-	-	200	$\Omega$
POWER SUPPLIES						
Positive Supply Current, $I_+$	$V_+ = 13.2V$ , $V_{IN} = 0V$ or $5V$	+25°C	-	0.001	1	$\mu A$
		Full	-	-	5	$\mu A$
Negative Supply Current, $I_-$	$V_{IN} = 0V$ or $5V$	+25°C	-1	-0.0001	-	$\mu A$
		Full	-5	-	-	$\mu A$
Logic Supply Current, $I_L$	$V_L = 5.25V$ , $V_{IN} = 0V$ or $5V$	+25°C	-	0.001	1	$\mu A$
		Full	-	-	5	$\mu A$
Ground Current, $I_{GND}$	$V_{IN} = 0V$ or $5V$	+25°C	-1	-0.001	-	$\mu A$
		Full	-5	-	-	$\mu A$

**NOTES:**

1. Signals on  $S_X$ ,  $D_X$ , or  $IN_X$  exceeding  $V_+$  or  $V_-$  will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. All leads welded or soldered to PC Board.
3.  $V_{IN}$  = input voltage to perform proper function.
4. Hot = as determined by the operating temperature suffix.
5. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
7. Guaranteed by design, not subject to production test.

Typical Performance Curves

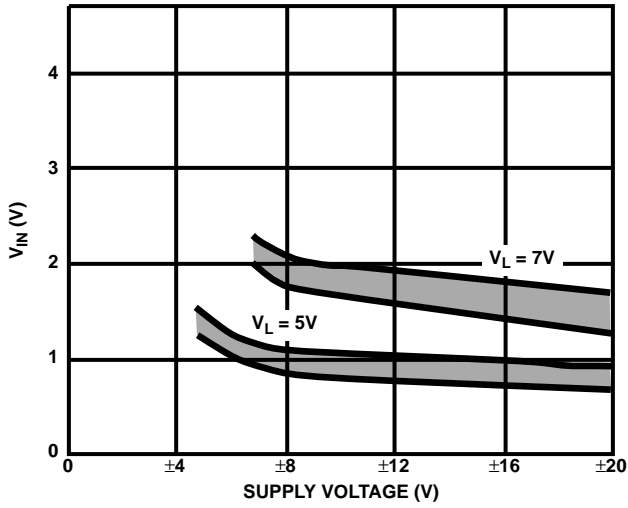


FIGURE 1. SWITCHING THRESHOLD vs SUPPLY VOLTAGE

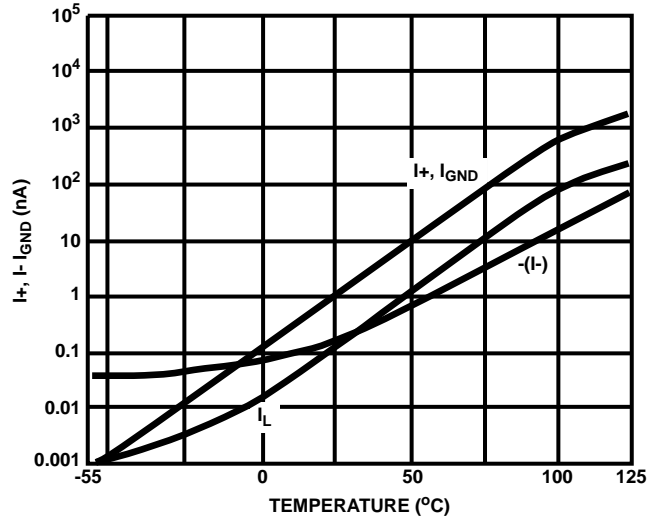


FIGURE 2. SUPPLY CURRENT vs TEMPERATURE

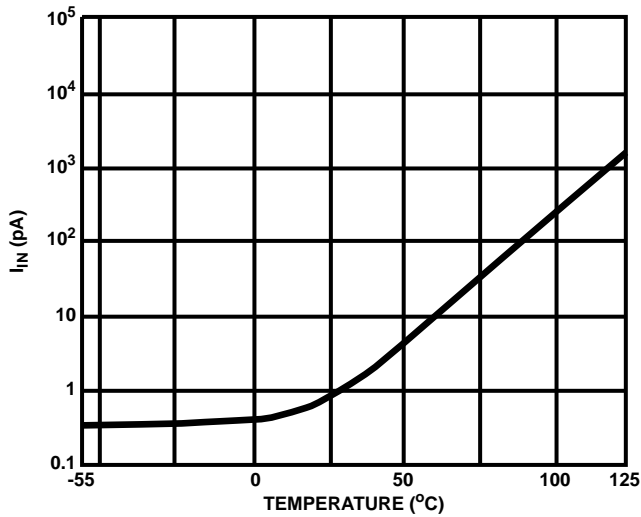


FIGURE 3. INPUT CURRENT vs TEMPERATURE

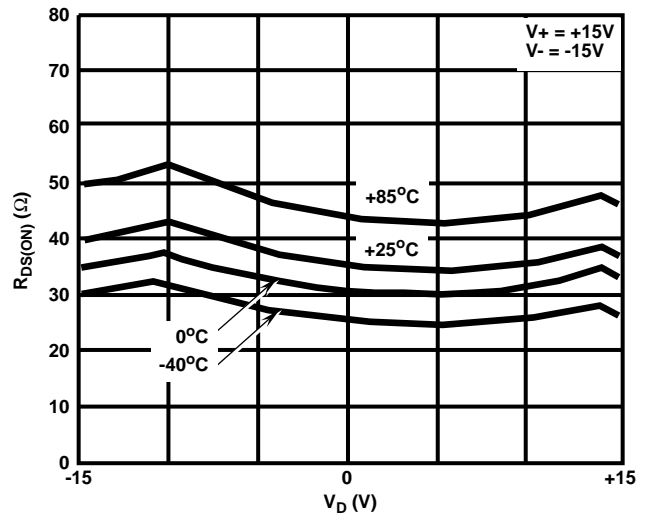


FIGURE 4.  $R_{DS(ON)}$  vs  $V_D$  AND TEMPERATURE

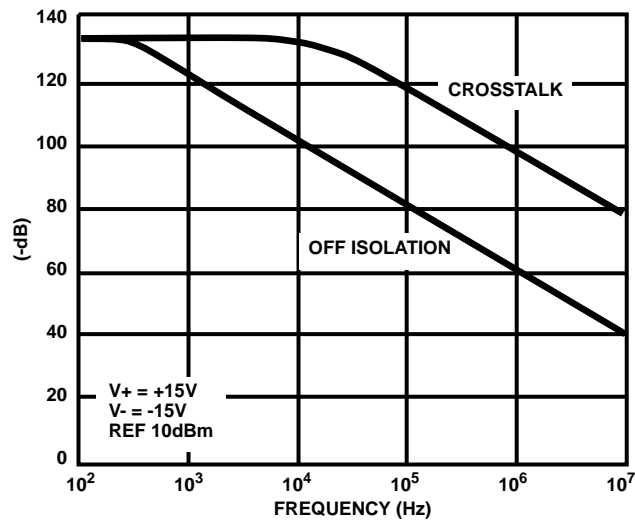


FIGURE 5. CROSSTALK AND OFF ISOLATION vs FREQUENCY

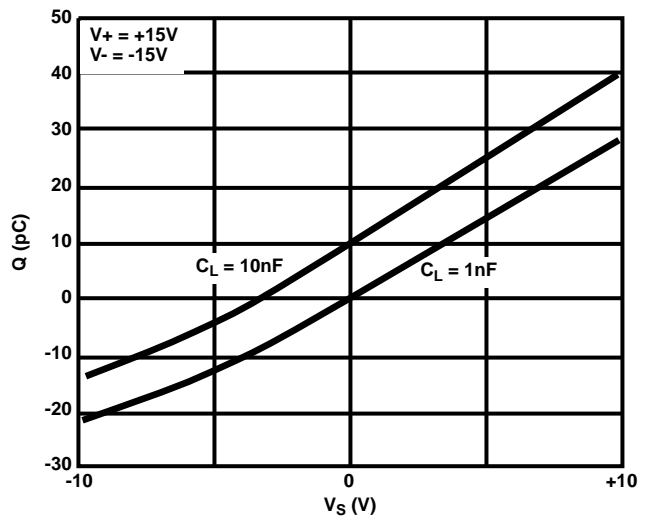


FIGURE 6. CHARGE INJECTION vs SOURCE VOLTAGE

Typical Performance Curves (Continued)

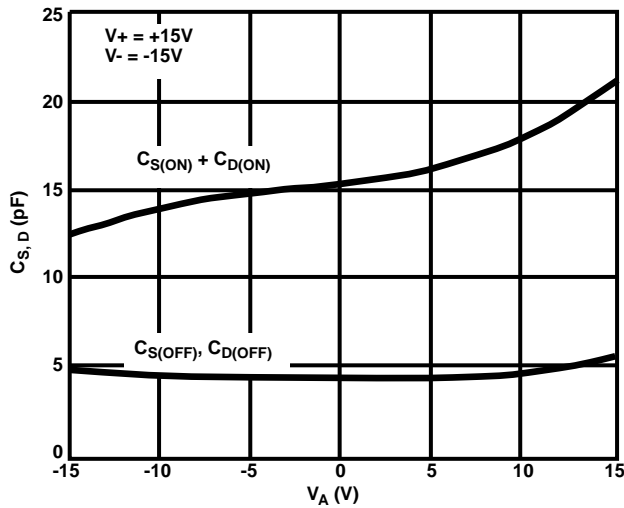


FIGURE 7. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE

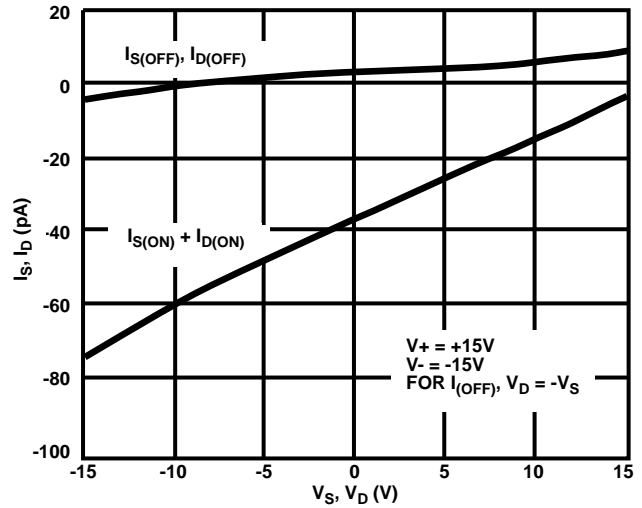


FIGURE 8. SOURCE/DRAIN LEAKAGE CURRENTS

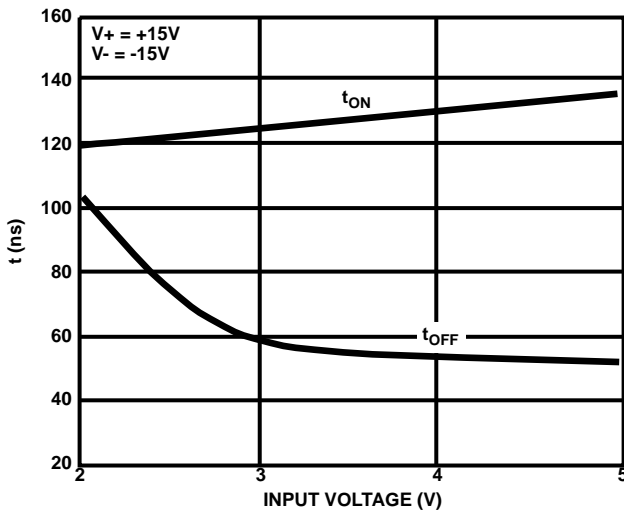


FIGURE 9. SWITCHING TIME vs INPUT VOLTAGE

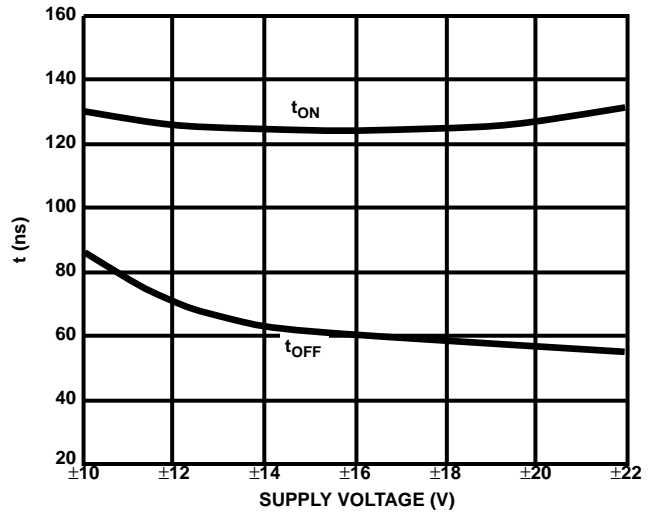


FIGURE 10. SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG444)

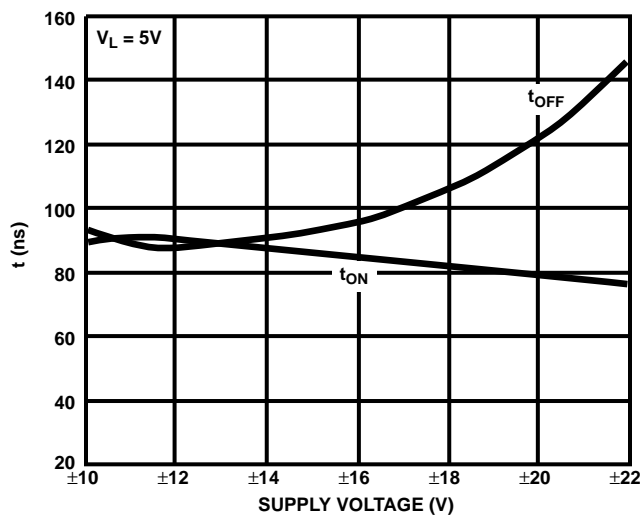


FIGURE 11. SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG445)

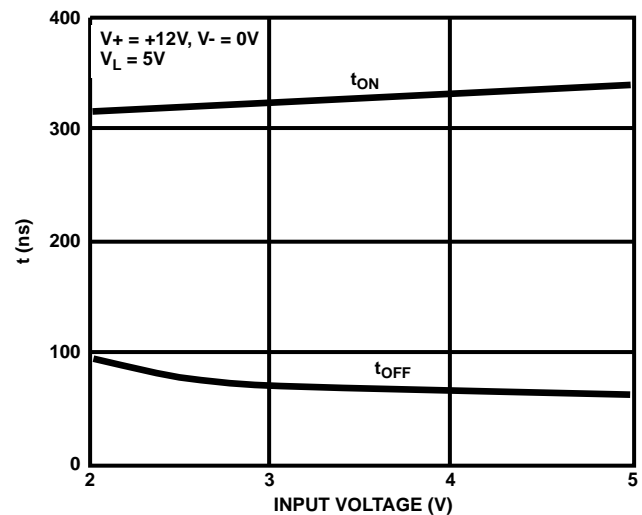


FIGURE 12. SWITCHING TIME vs INPUT VOLTAGE (DG444)

Typical Performance Curves (Continued)

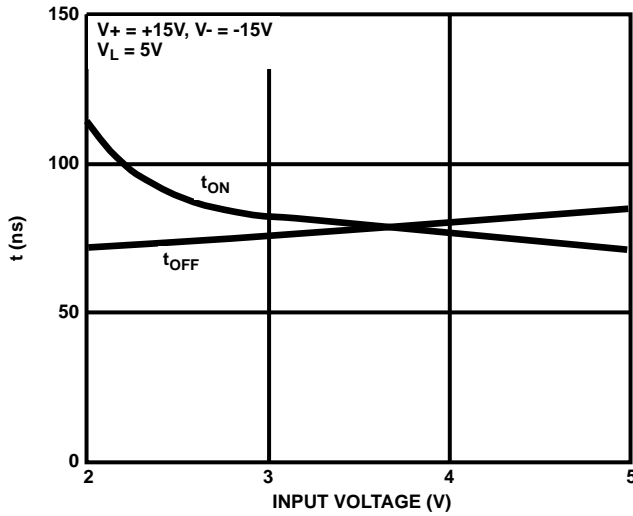


FIGURE 13. SWITCHING TIME vs INPUT VOLTAGE (DG445)

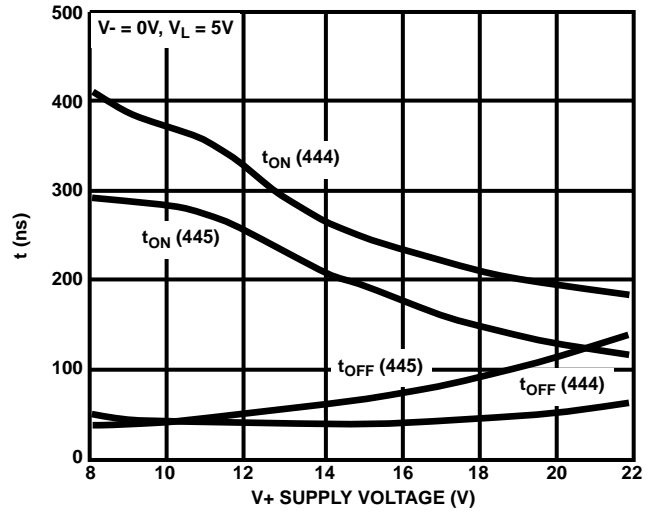


FIGURE 14. SWITCHING TIMES vs POWER SUPPLY VOLTAGE

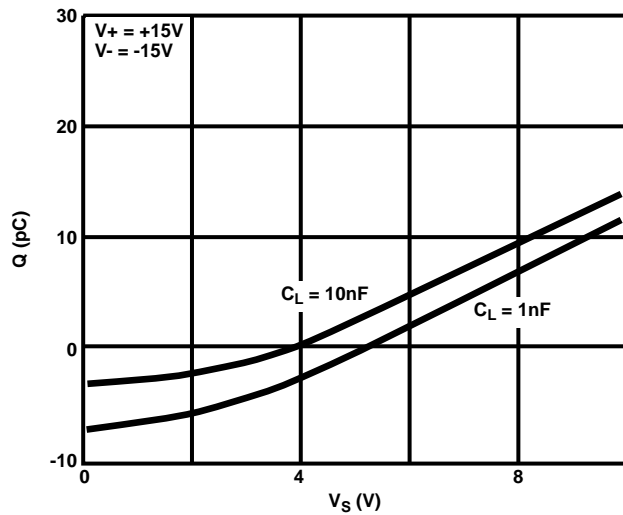


FIGURE 15. CHARGE INJECTION vs SOURCE VOLTAGE (SINGLE 12V SUPPLY)

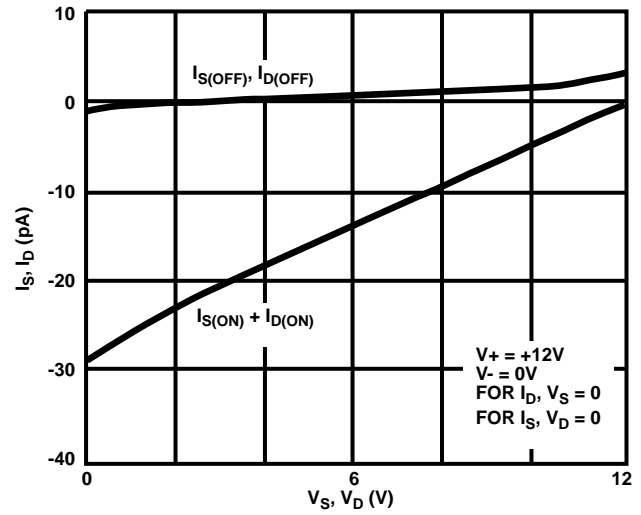


FIGURE 16. SOURCE/DRAIN LEAKAGE CURRENTS (SINGLE 12V SUPPLY)

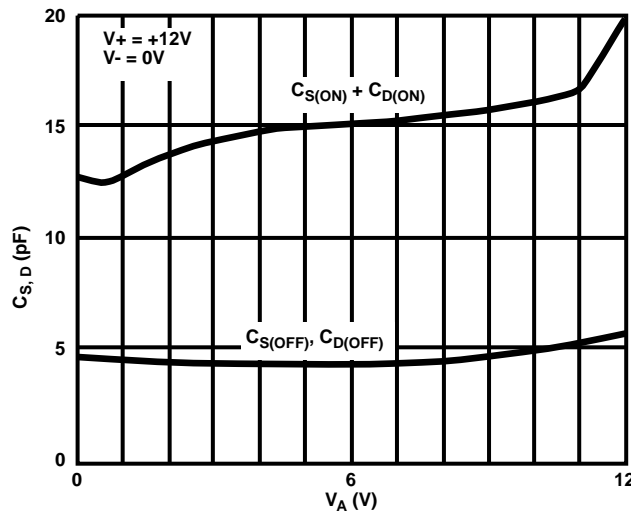


FIGURE 17. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE (SINGLE 12V SUPPLY)

**Pin Description**

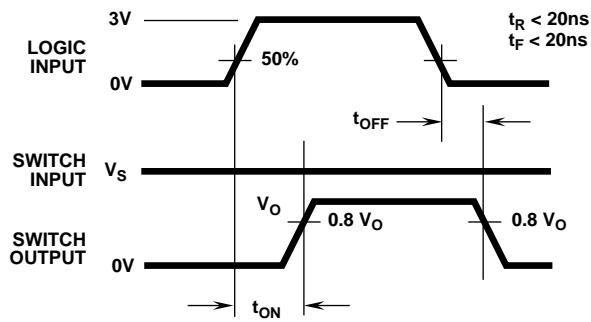
PIN	SYMBOL	DESCRIPTION
1	IN <sub>1</sub>	Logic control for switch 1
2	D <sub>1</sub>	Drain (output) terminal for switch 1
3	S <sub>1</sub>	Source (input) terminal for switch 1
4	V-	Negative power supply terminal
5	GND	Ground terminal (Logic Common)
6	S <sub>4</sub>	Source (input) terminal for switch 4
7	D <sub>4</sub>	Drain (output) terminal for switch 4
8	IN <sub>4</sub>	Logic control for switch 4
9	IN <sub>3</sub>	Logic control for switch 3
10	D <sub>3</sub>	Drain (output) terminal for switch 3
11	S <sub>3</sub>	Source (input) terminal for switch 3
12	V <sub>L</sub>	Logic reference voltage.
13	V+	Positive power supply terminal (substrate)
14	S <sub>2</sub>	Source (input) terminal for switch 2
15	D <sub>2</sub>	Drain (output) terminal for switch 2
16	IN <sub>2</sub>	Logic control for switch 2

**TRUTH TABLE**

LOGIC	V <sub>IN</sub>	DG444	DG445
0	≤0.8V	ON	OFF
1	≥2.4V	OFF	ON

**Test Circuits**

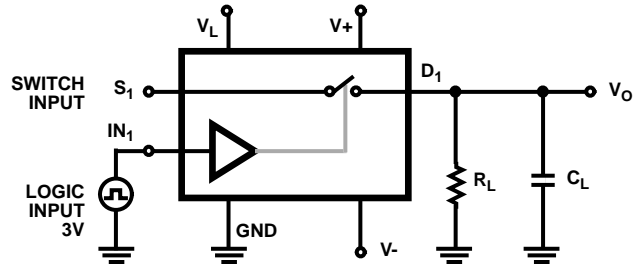
V<sub>O</sub> is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 18A.

FIGURE 18. SWITCHING TIME



Repeat test for Channels 2, 3 and 4.

For load conditions, see Specifications C<sub>L</sub> (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 18B.

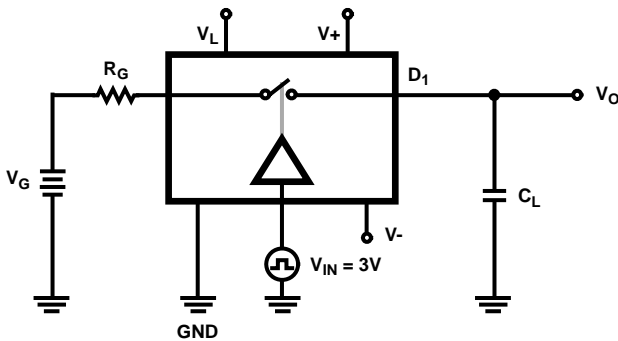


FIGURE 19A.

FIGURE 19. CHARGE INJECTION

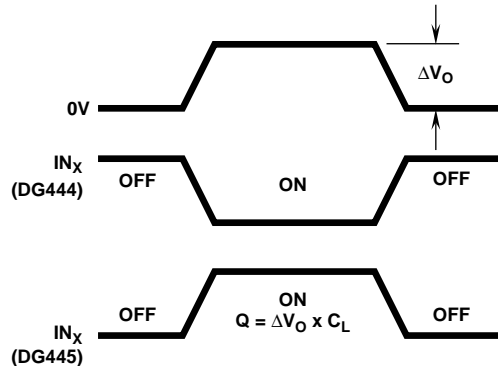


FIGURE 19B.



Test Circuits (Continued)

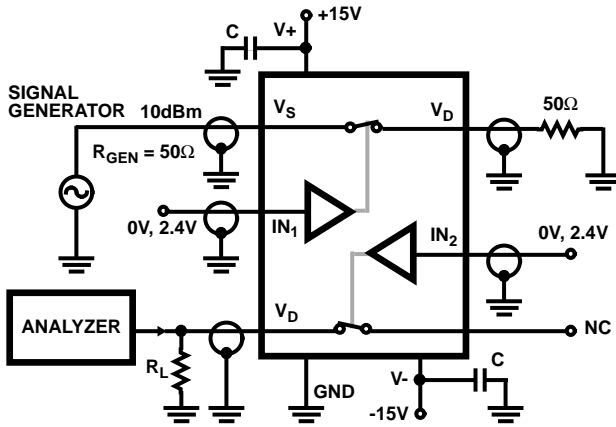


FIGURE 20. CROSSTALK

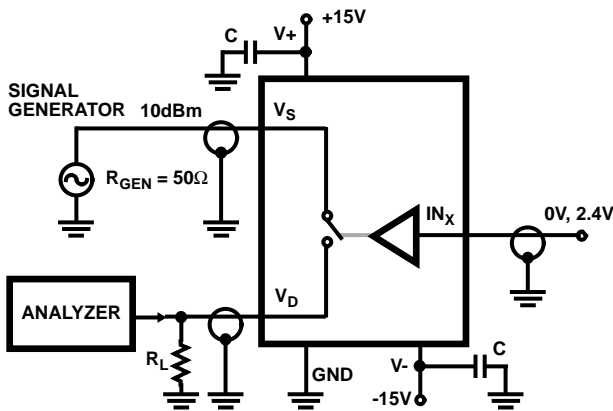


FIGURE 21. OFF ISOLATION

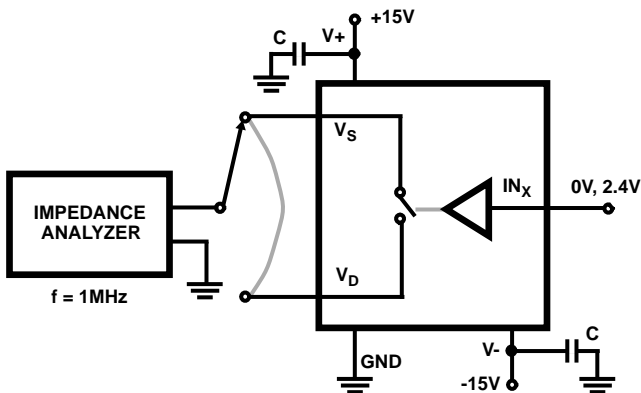
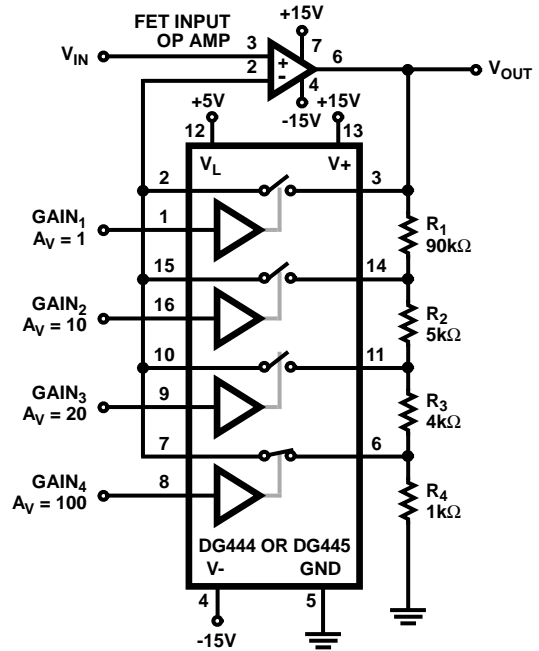


FIGURE 22. SOURCE/DRAIN CAPACITANCES

Typical Applications



GAIN ERROR IS DETERMINED ONLY BY THE RESISTOR TOLERANCE, OP AMP OFFSET AND CMRR WILL LIMIT ACCURACY OR CIRCUIT

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1 + R_2 + R_3 + R_4}{R_4} = 100$$

WITH SW<sub>4</sub> CLOSED

FIGURE 23. PRECISION WEIGHTED RESISTOR PROGRAMMABLE GAIN AMPLIFIER

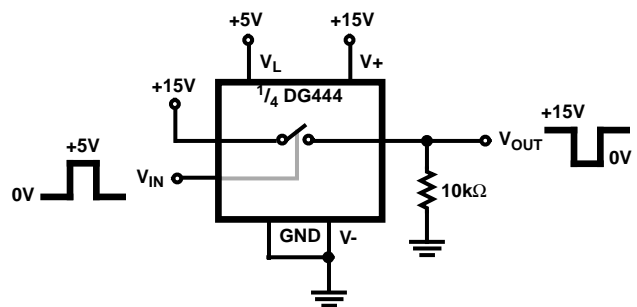


FIGURE 24. LEVEL SHIFTER

**Die Characteristics**

**DIE DIMENSIONS:**

2160 $\mu\text{m}$  x 1760 $\mu\text{m}$  x 485  $\pm$  25 $\mu\text{m}$

**METALLIZATION:**

Type: CuAl

Thickness: 12k $\text{\AA}$   $\pm$  1k $\text{\AA}$

**GLASSIVATION:**

Type: Nitride

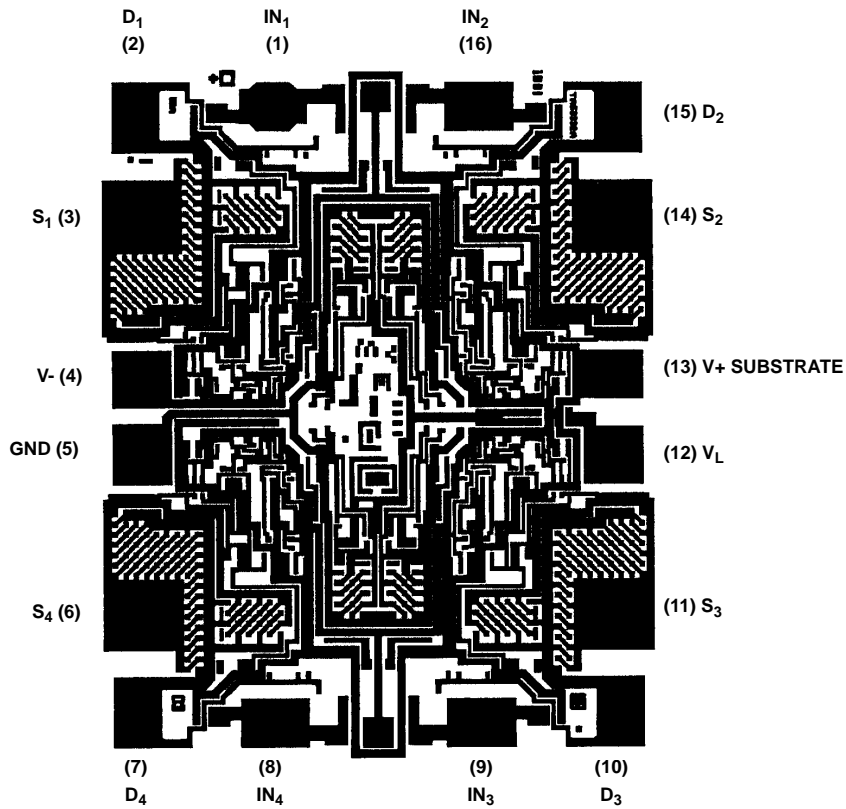
Thickness: 8k $\text{\AA}$   $\pm$  1k $\text{\AA}$

**WORST CASE CURRENT DENSITY:**

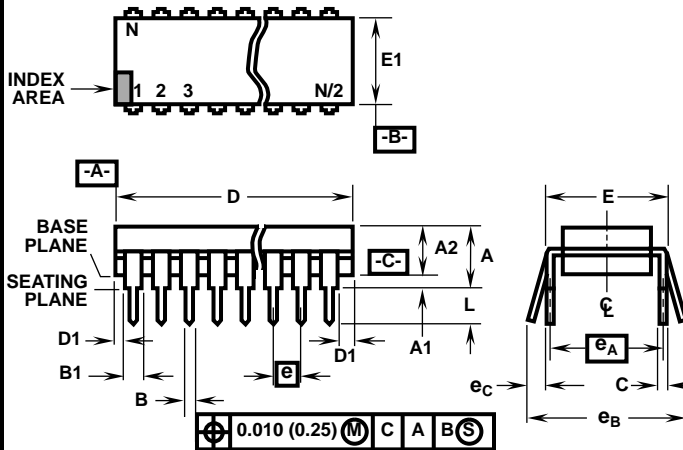
9.1 x 10<sup>4</sup>A/cm<sup>2</sup>

**Metallization Mask Layout**

DG444, DG445



Dual-In-Line Plastic Packages (PDIP)



E16.3 (JEDEC MS-001-BB ISSUE D)  
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

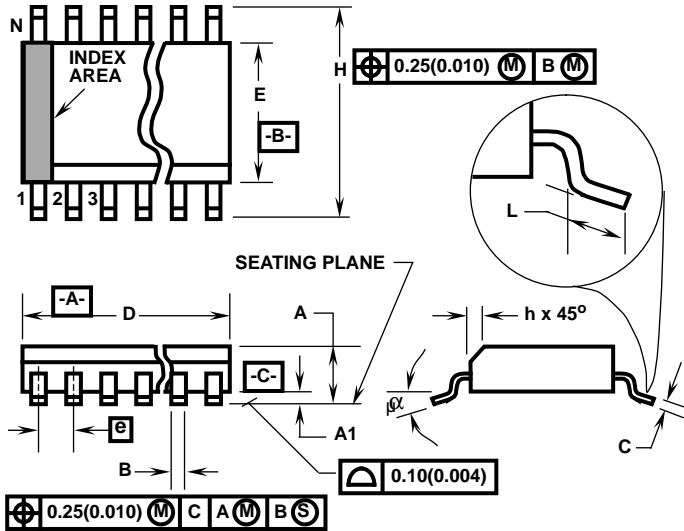
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e <sub>A</sub>	0.300 BSC		7.62 BSC		6
e <sub>B</sub>	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

NOTES:

- Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- E and e<sub>A</sub> are measured with the leads constrained to be perpendicular to datum -C-.
- e<sub>B</sub> and e<sub>C</sub> are measured at the lead tips with the leads unconstrained. e<sub>C</sub> must be zero or greater.
- B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Rev. 0 12/93

**Small Outline Plastic Packages (SOIC)**



**M16.15 (JEDEC MS-012-AC ISSUE C)**  
**16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
$\alpha$	0°	8°	0°	8°	-

**NOTES:**

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 0 12/93

*Harris Semiconductor products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Harris is believed to be accurate and reliable. However, no responsibility is assumed by Harris or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Harris or its subsidiaries.*

**Sales Office Headquarters**

For general information regarding Harris Semiconductor and its products, call **1-800-4-HARRIS**

**UNITED STATES**

Harris Semiconductor  
 2401 Palm Bay Road N.E.  
 Palm Bay, Florida 32905  
 TEL: (407) 724-7000

**EUROPE**

Harris Semiconductor  
 Mercure Center  
 100, Rue de la Fusee  
 1130 Brussels, Belgium  
 TEL: (32) 2-724-2111

**SOUTH ASIA**

Harris Semiconductor H.K. Ltd.  
 13/F Fourseas Building  
 208-212 Nathan Road  
 Tsimshatsui, Kowloon  
 Hong Kong  
 TEL: (852) 723-6339

**NORTH ASIA**

Harris K.K.  
 Kojimachi-Nakata Bldg. 4F  
 5-3-5 Kojimachi  
 Chiyoda-ku, Tokyo 102 Japan  
 TEL: (81) 3-3265-7571  
 TEL: (81) 3-3265-7572 (Sales)

